Circuit Architecture for VTL with MLC Flash Transistor

Fig. 1A

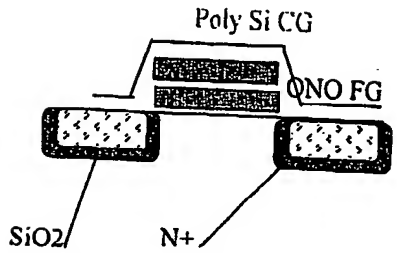


Fig. 1A'

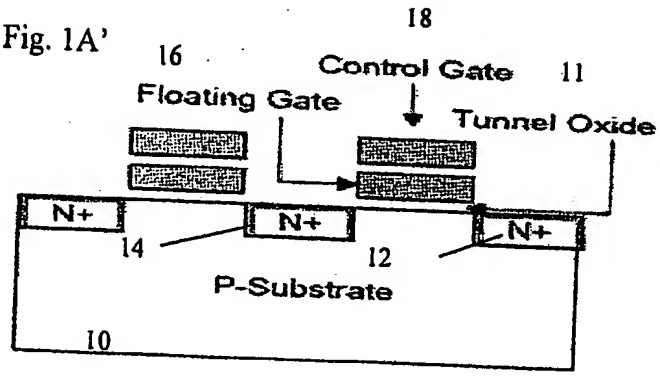


Fig. 1C

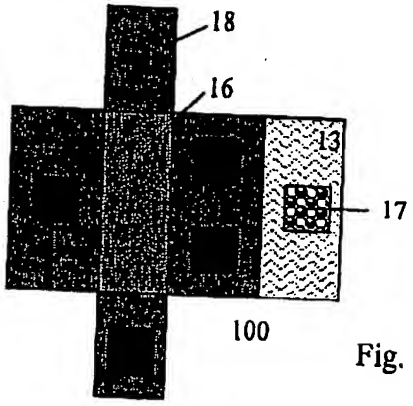
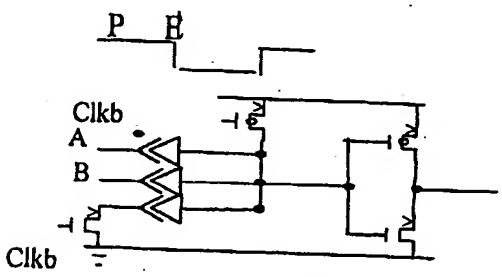


Fig. 1B



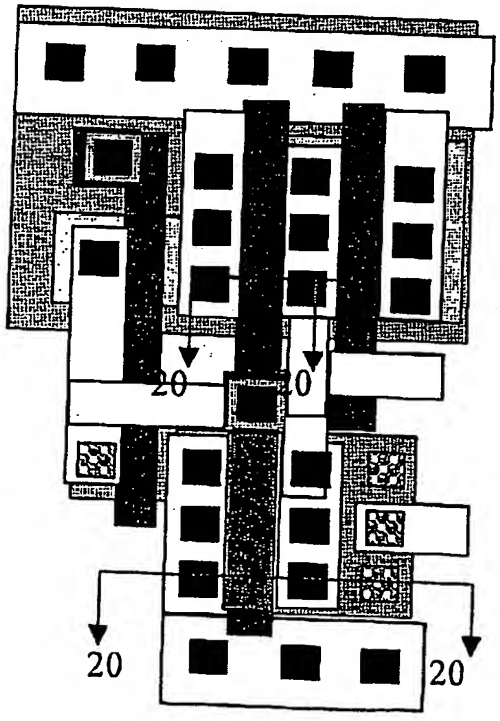


Fig. 1E

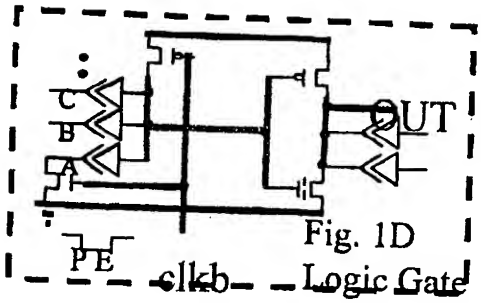


Fig. 1D

System architecture of VTL and MLC arrays

Fig. 2

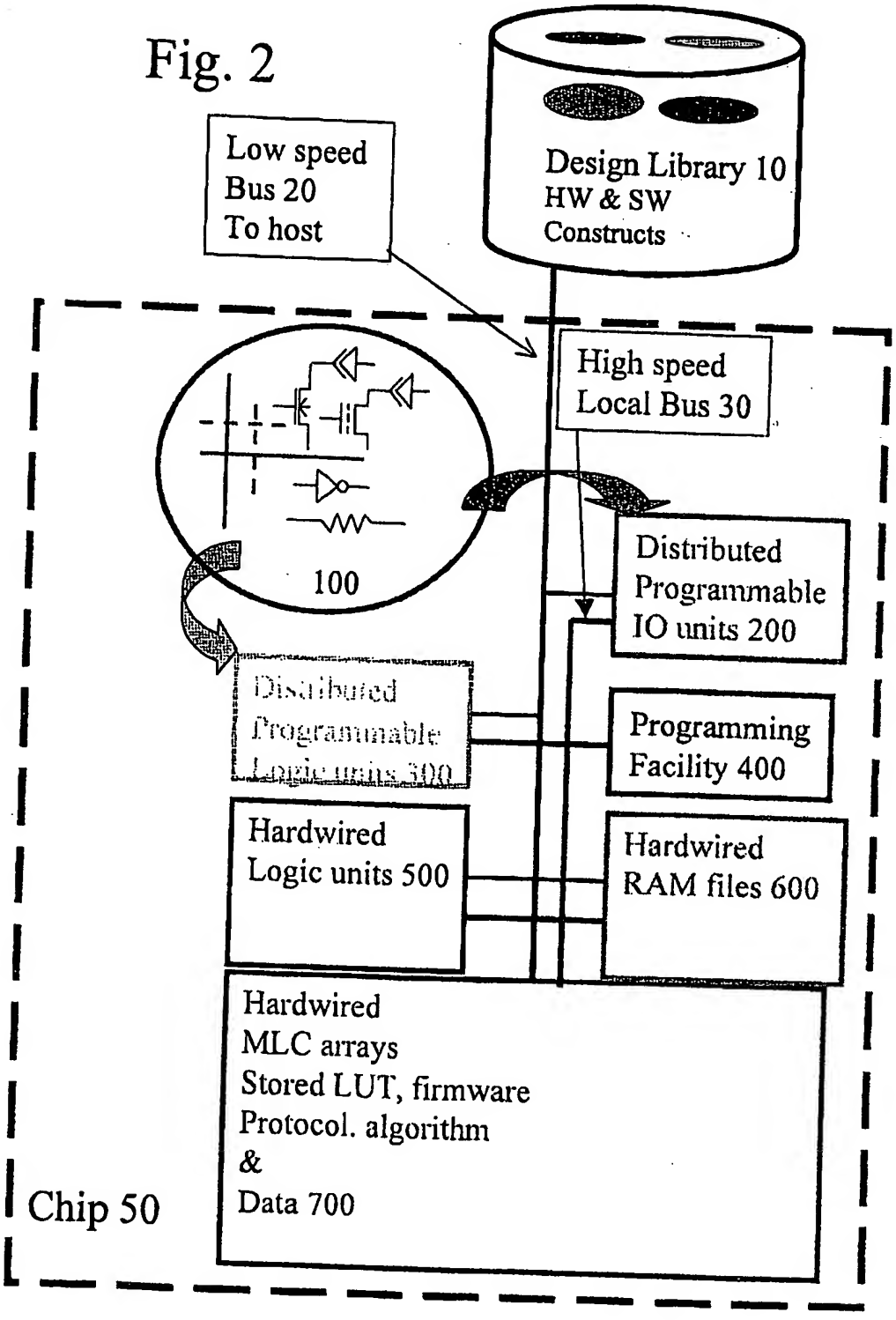
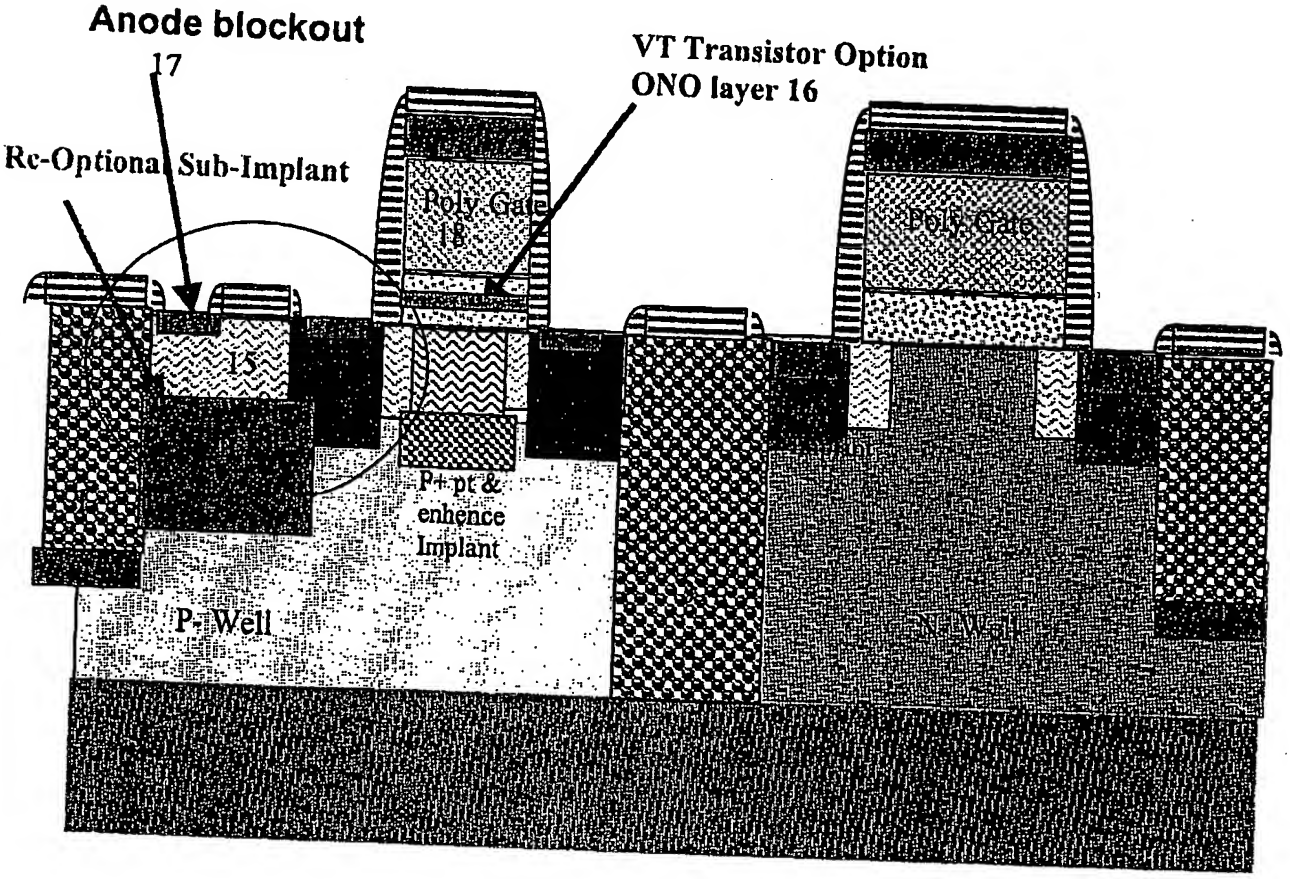


Fig. 3

- Integrated Schottky-CFET cross section view
- ***SBD special:*** Anode implant block out, barrier metal, and Cathode bulk resistance implant

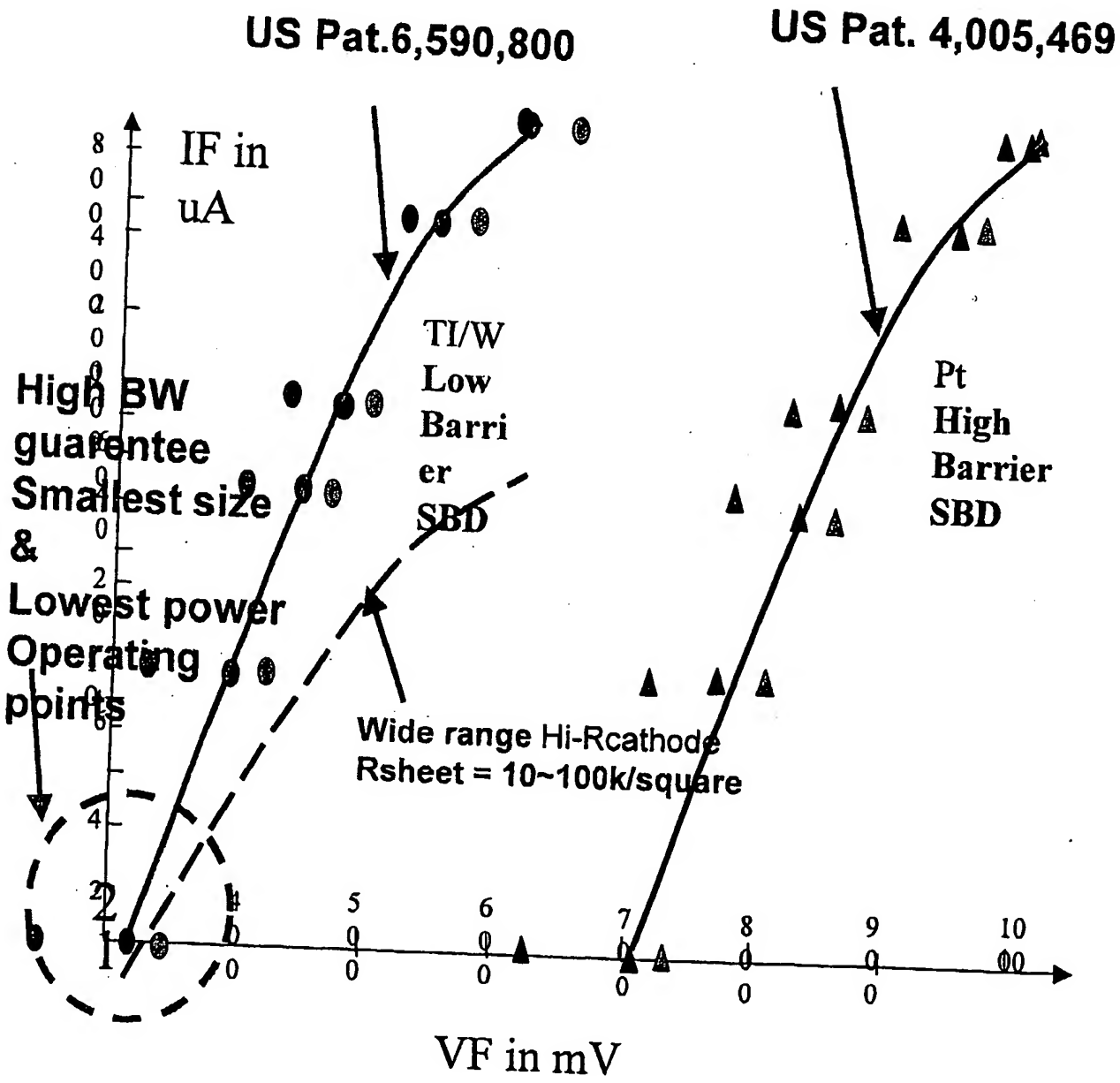


Standard processes: Conventional Trench/ROX Isolation, CMOS transistors, and post contact metal processes

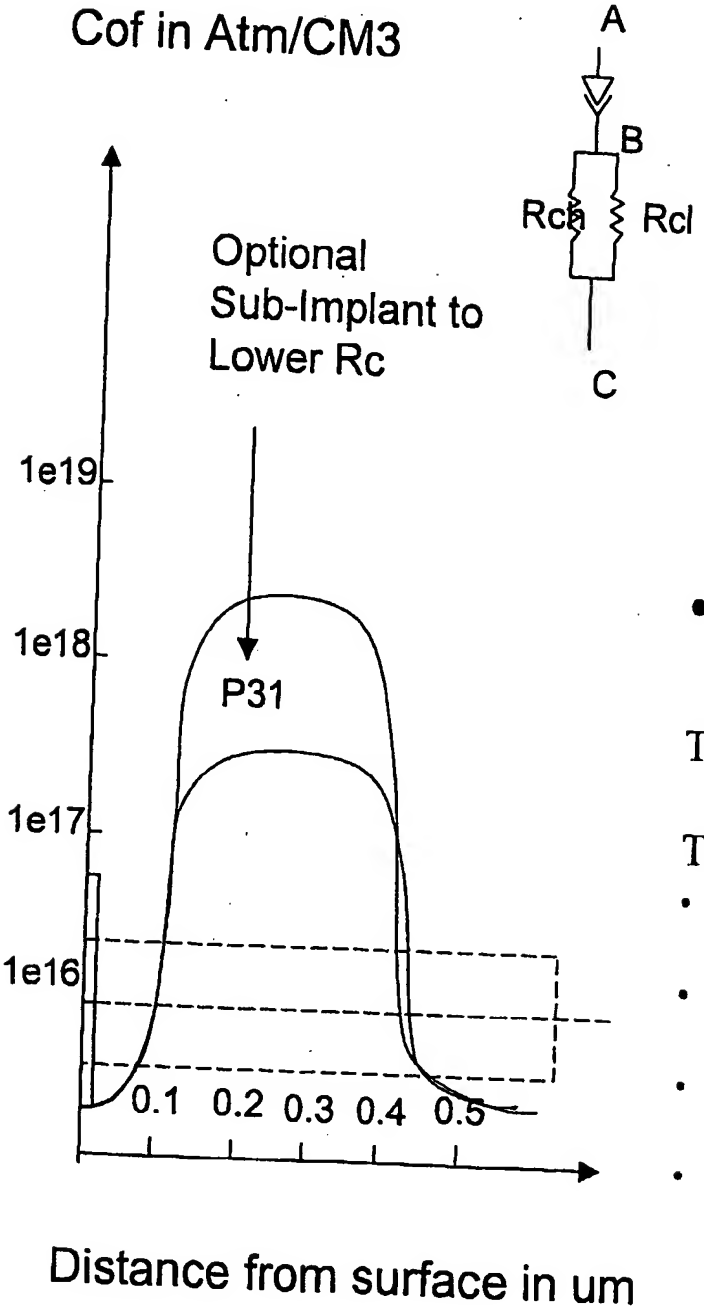
SBD IF vs VF

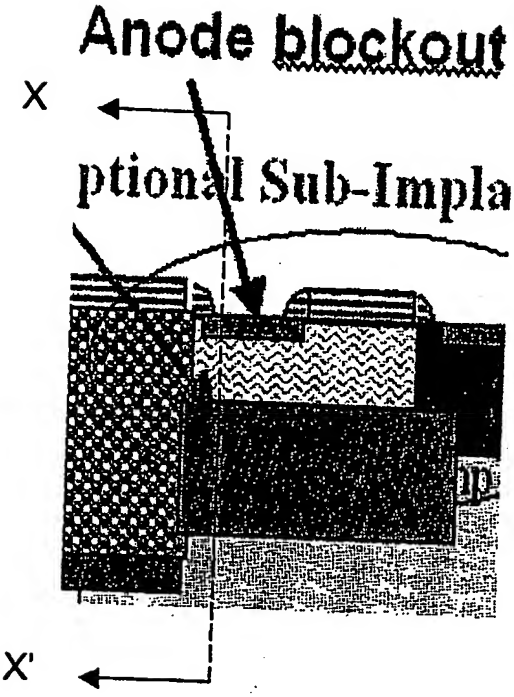
Fig. 4

- Diode curves at –0, 25, 85 oC junction
- R~1.5KΩ for I<100 uA, R~150Ω for I<1 mA



, SBD Rc effect





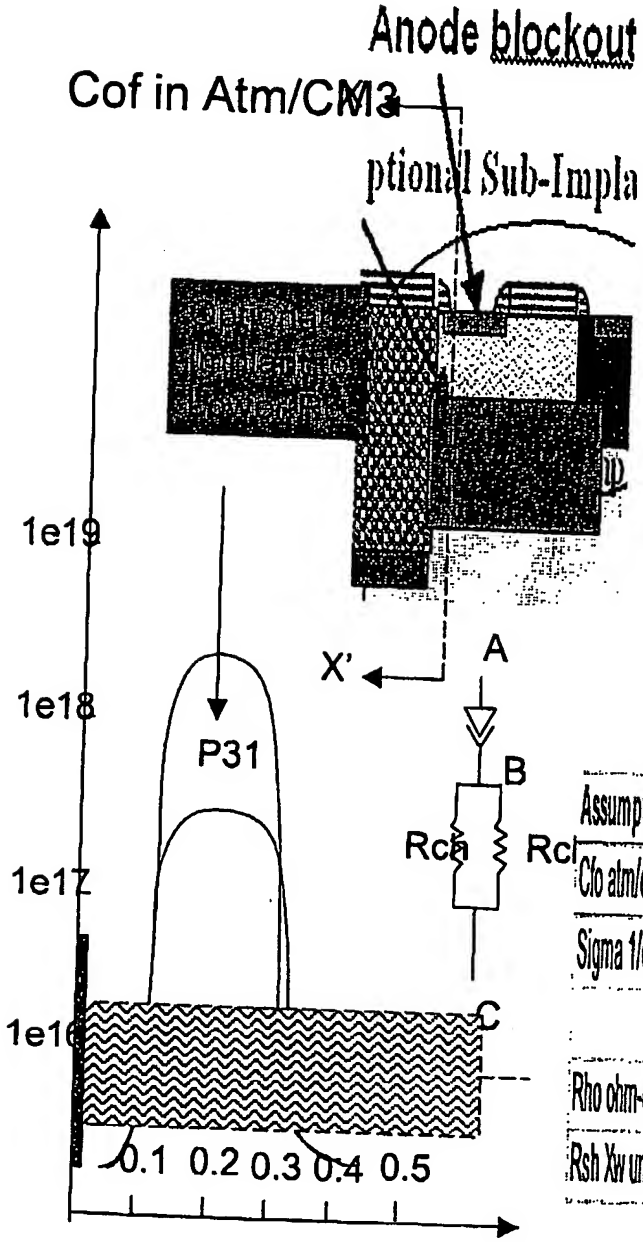
- SBD Device Structures

The Anode is formed by Metal-Si compound--Ti3Si4

The Cathode has two segments

- Tch is the high sheet rho part-several **Kohm/sq**
- Tch may be formed by epi or low dosage Implant~10^{16} atm/cm^3
- **Tcl is the low sheet rho part <100 ohm/sq**
- **Tcl may be formed by epi with barried diffusion or high dosage Sub-Implant~10^{18} atm/cm^3**

SBD Rc effect 2



The Rc effect					
Assumption: W/O sub Implant, from Irvin					
Cfo atm/cm3		1.00E+15	5.00E+15	1.00E+16	5.00E+16
Rho ohm-cm		4.7	1.1	0.6	0.15
Dfo um	0.1	47000	11000	6000	1500
Rsh-Ohm/sq=Rho/Dfo	0.2	23500	5500	3000	750
	0.3	15666.667	3666.6667	2000	500

Fig. 5

Assumption: With sub-Implant, Gaussian							
Cfo atm/cm3		1.00E+15	5.00E+15	1.00E+16	5.00E+16	1.00E+17	1.00E+18
Sigma 1/ohm-cm	Nbc=1e15		0.4	0.8	3	5	20
	Nbc=1e17			0.2	0.8	2	6
Rho ohm-cm	Nbc=1e15		2.5	1.25	0.333333	0.2	0.05
Rsh Xw um	0.2		12500	6250	1667	1000	250
	0.4		6250	3125	833	500	125
	0.6		4167	2083	556	333	83

Fig. 6A Open Reference literature

Today, advanced wafer packaging processes al Hewlett-Packard to ma low cost surface moun diodes in high volumes mercial and consumer applications. Tradition of these diodes are use ing and power monitor applications such as in cordless phones, satell sion receivers, RFID (r frequency identificatio and many others. How creasing number of the are also used in digital applications such as th of transistor, optocoup erational amplifier circ over-voltage protectior and clamping.

When the Schottky diode is reversed biased, the potential barrier for electrons becomes large: hence there is a small probability that an electron will have sufficient thermal energy to cross the junction. The reverse leakage current will be in the nanoampere range.

In contrast to a conventional p-n junction, current in the Schottky diode is carried only by majority carriers. Because no minority carrier charge storage effects are present, Schottky diodes have carrier lifetimes of less than 100 ps and are extremely fast switching semiconductors.

Another significant diffe tween Schottky and p-n voltage drop des have a t 3 V compar nction diod

careful man er of the Sc he choice o the n-doped aracteristic on capacita es resistanc oltage V_{br} a

Table 1.

Parameter	HSMS-280X	HSMS-282X
C_{jo}	1.6	0.7
V_{br}	75	9
R_s	30	5
E_c	0.69	0.69
I_{BV}	10.0E-6	10.0E-4
I_s	3.0E-8	2.2E-8
N	1.08	1.08
P_B	0.65	0.65
P_T	2	2
M	0.5	0.5

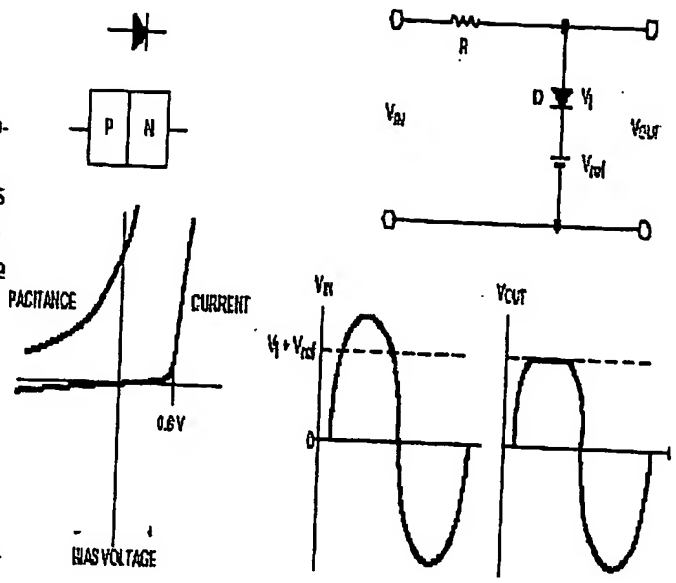


Figure 4.

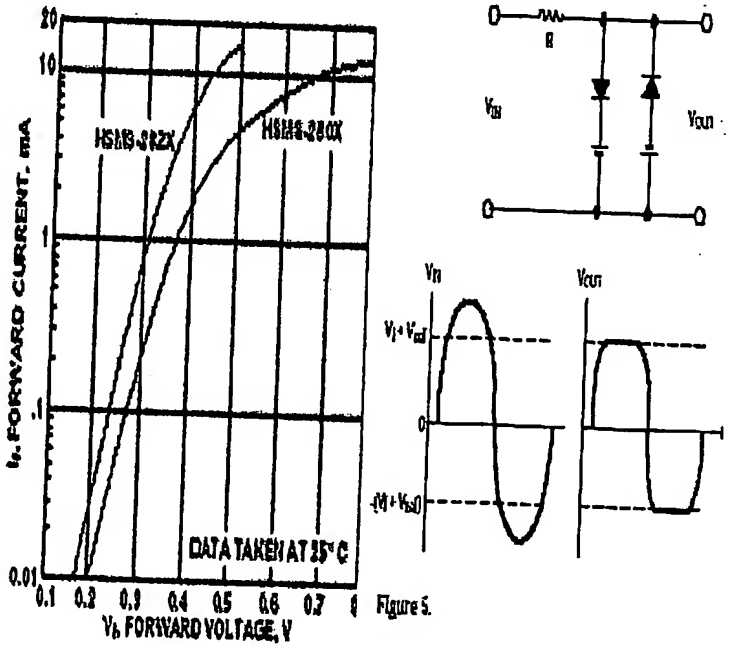


Figure 5.

Figure 2. Forward Current vs. Forward Voltage.

Fig. 6B Reference literature

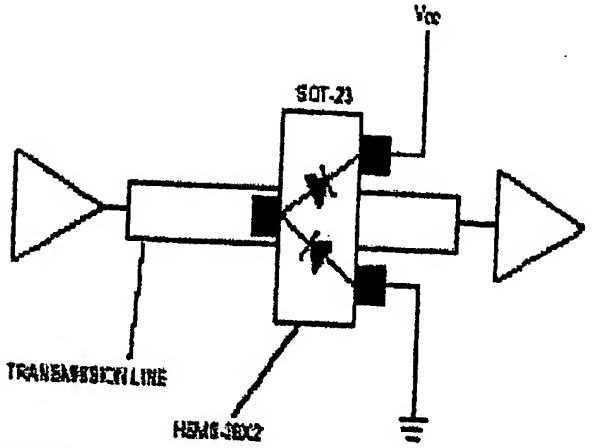


Figure 6.

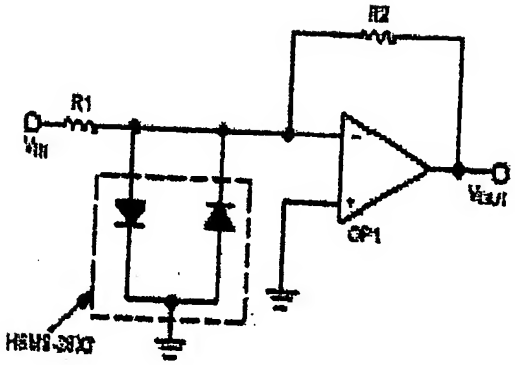


Figure 7.

Protection and Improving Performance of Operational Amplifiers

Operational amplifier input overload, which can occur in the form of excessive common-mode or differential voltages, can result in a voltage breakdown that will damage or destroy the input transistors of the device.

Amplifier Protection

Protection of an operational amplifier from high input voltages can be achieved by using a series diode (HSMS 28X2) as shown in Figure 7. The diodes limit the voltages at the input to the operational amplifier to safe levels (approx. 0.4 V) without restricting the signal swing.

Settling Time Speedup

An important consideration for operational amplifier performance

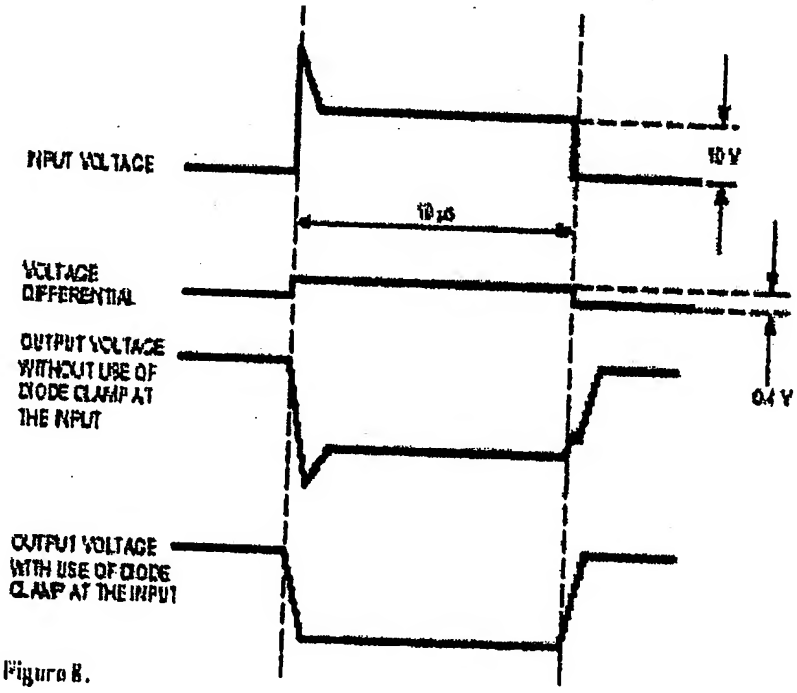


Figure 8.

age, $V_3 - V_2$. Since the integration circuit typically has a slow response time, it cannot respond to fast input spikes, thus resulting in ringing in the output signal and

cellent choice for a variety of non-RF applications. For further information, contact your local Hewlett-Packard sales office.

Fig. 7 *5th Gen. IC, Schottky-CMOS-Logic (SCL™)*

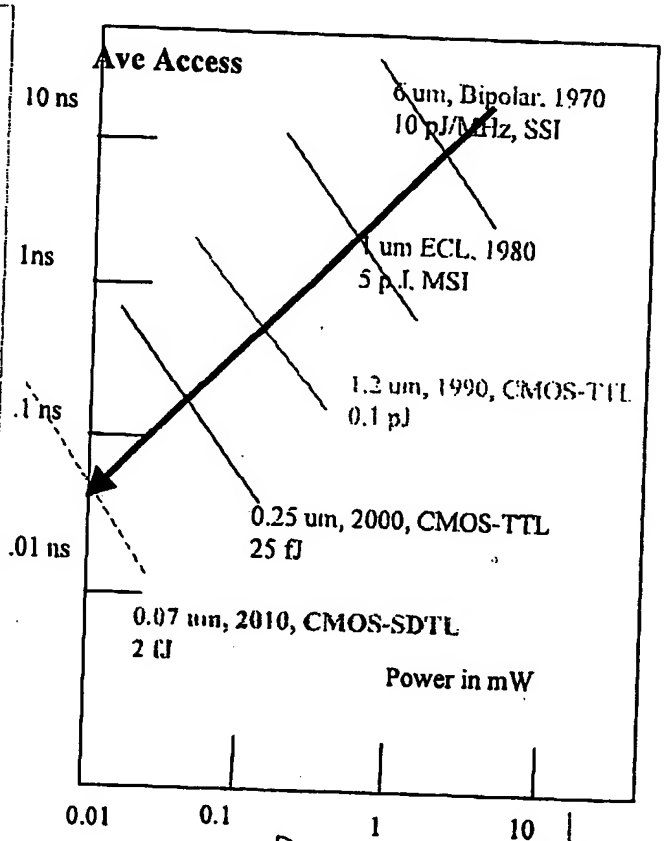
邏輯线路的優越性

IC circuit solution and cost trends

Figure of merit index comparison on NAND4 gate

	Area	Access time	Powe	Defect	AAP Cost
Bipolar TTL	100	100	100	100	1E8
Bipolar ECL 1985	200	10	200	200	8E7
CMOS TTL 2000	10	10	10	10	1E4
CMOS-SDTL 2004	2	2	2	2	16

	Bipolar		CMOS		
Tech rules/pars	1970	1980	1990	2000	2 010
Gox/Wb Ang	4000	2000	200	70	50
H um left	6	3	1	0.25	0.07
H um film	1	0.5	0.4	0.3	0.2
Contactspace um	10	2	1.2	0.25	0.2
Typ C load in F	10pF	1pF	0.4pF	200fF	50fF
Op. V volt	8	5	3.3	2.5	1.2
Op. I mA CV*f	1	0.1	.01	1uA	10 nA
Speed nS	70	10	3	500 pS	200 pS
Power*Speed pJ	560	5	0.1	0.03	1.3 fJ
W inch	3.5	4	6	8	12
Density Gates	100	2000	20k	200k	1M



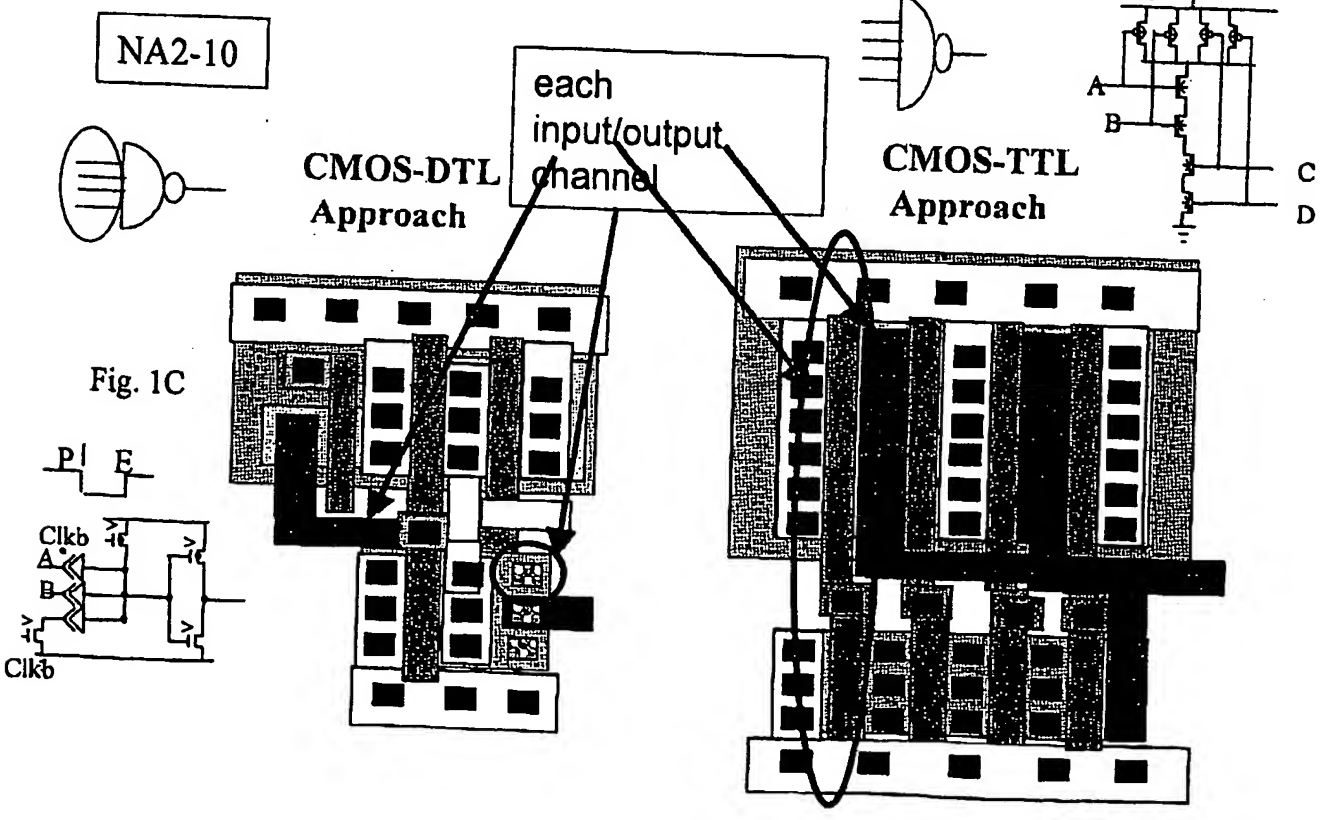


Fig. 1C

Fig. 8 Demonstrative Embedded Library Solutions

Exemplary logic applications additional to MLC arrays

Low power IO Block functions

- ESD clamp diodes and line terminators
- Schmitt trigger at 1.2V
- ZBUF 1.2V
- Transceivers 1.2V

Low power internal logic and level shifter

- Inverter, NAND, NOR, DFF, and combinationals.
- XOR4
- Analog Differential Sense Amp and latch 1, 2

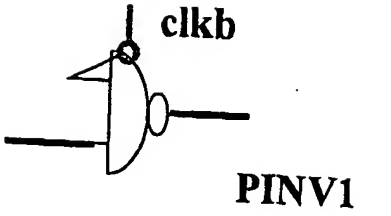
Special functions

1. Oscillators
2. PLL and DLL
3. High speed RAM
4. Mask ROM, OTP and FPGA
5. Arithmetic; Adder + Multiplier
6. Absolute value function
7. ADC/DAC

Controller Applications

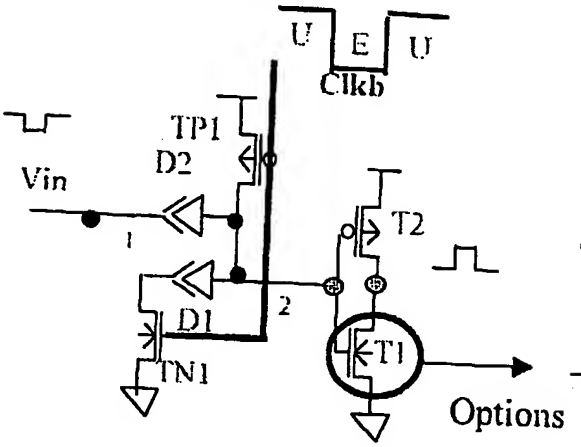
- Semiconductor Disks
- Image storage and access devices
- Network storage and access devices
- Wireless and mobile communications
- Multimedia interfaces and data transports
- Generic Programmable computing devices

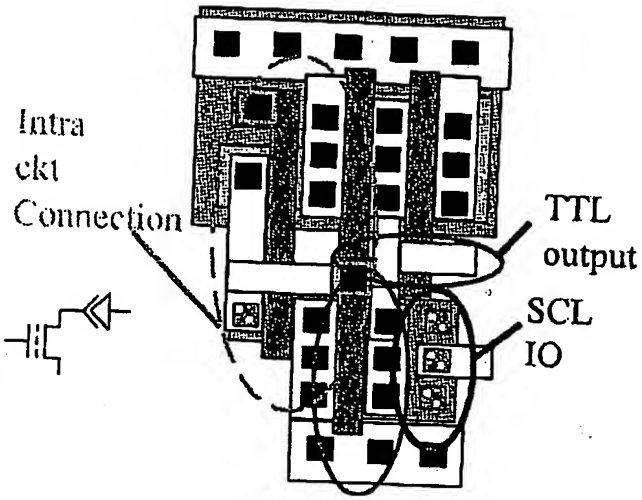
Fig. 9 Pulsed INV

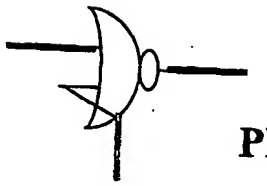


PINV1

Vin	Clkb	Vo
X	H	H
1	L	0
0	L	1

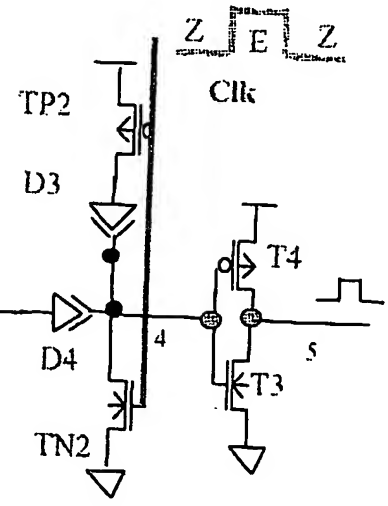






PINV2

Vin	Clk	Vo
X	L	L
1	H	0
0	H	1



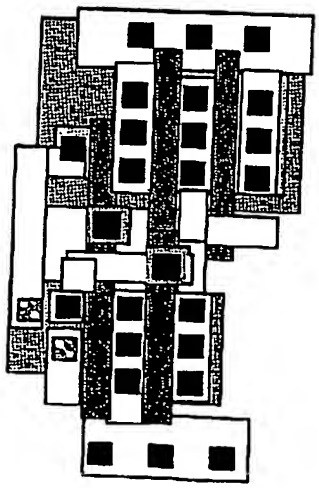
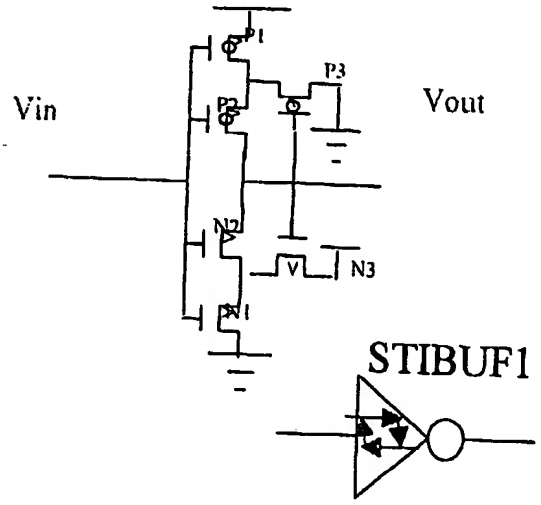
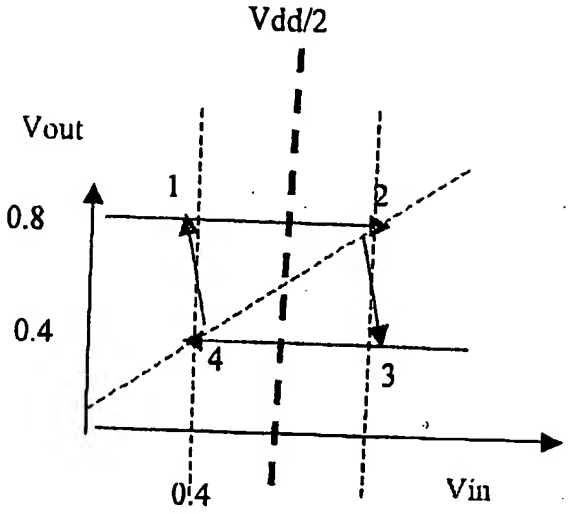


Fig. 10 Lo Power STIBUF

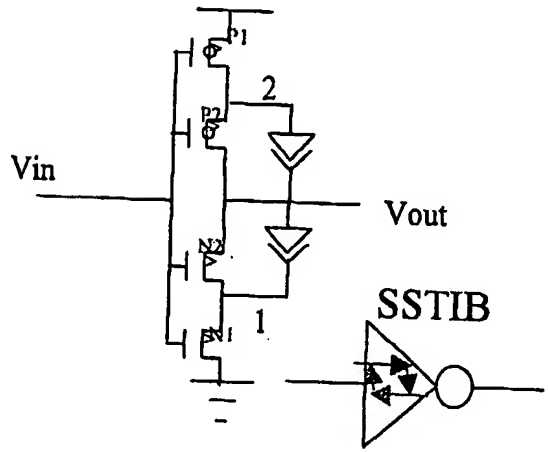
Schmitt Trigger- for VDD=1.2-1.5V, Different Input Vt

- **VtLH=0.8V**
- **VtHL=0.4V**

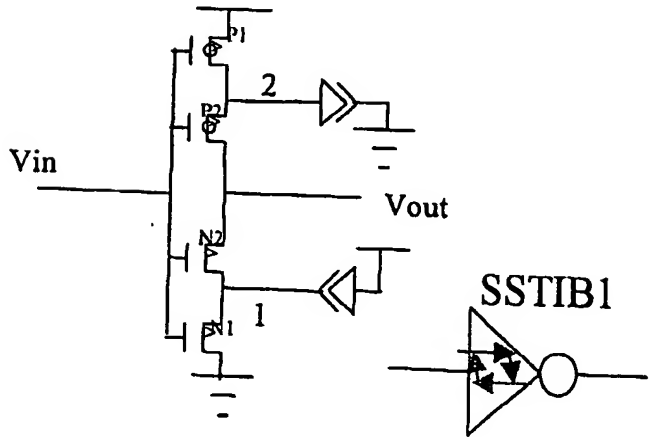




0.8



•	Vin	V1	V2	Vout
1.	0	1.2	1.5	1.5
2.	0.4	1.2	1.5	1.5
3.	0.6	1.2	1.5	1.5
4.	0.8	0.5	1.1	0.8
5.	1.2	0	0.3	0
6.	1.5	0	0	0
7.	1.2	0	0.3	0
8.	0.8	0.5	1.1	0.8
9.	0.4	1.2	1.5	1.5
10.	0	1.2	1.5	1.5



•	Vin	V1	V2	Vout
1.	0	1.2	1.5	1.5
2.	0.4	1.2	1.5	1.5
3.	0.6	1.2	1.5	1.5
4.	0.8	0.5	1.1	0.8
5.	1.2	0	0	0
6.	1.5	0	0	0
7.	1.2	0	0	0
8.	0.8	0	1.0	1.3
9.	0.4	1.2	1.5	1.5
10.	0	1.2	1.5	1.5

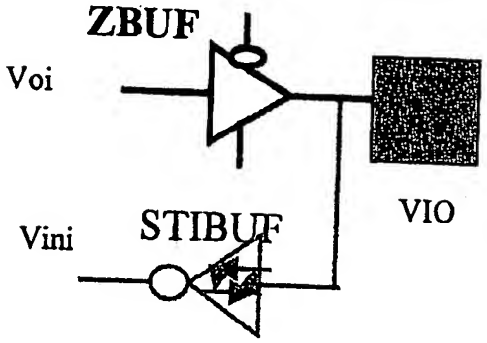
Fig. 11 Lo Power IOBUF

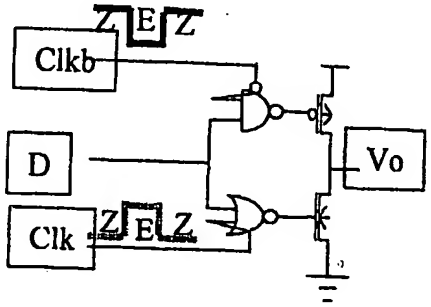
Single Phase Schmitt Trigger-
VDD=1.2-1.5V
Different Input Vt

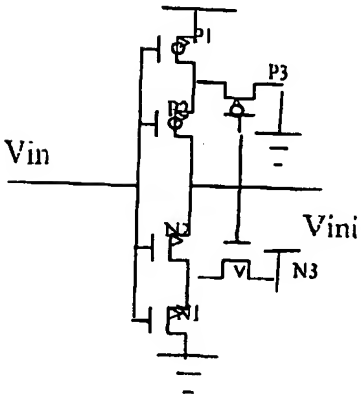
- **VtLH=0.8V**
- **VtHL=0.4V**

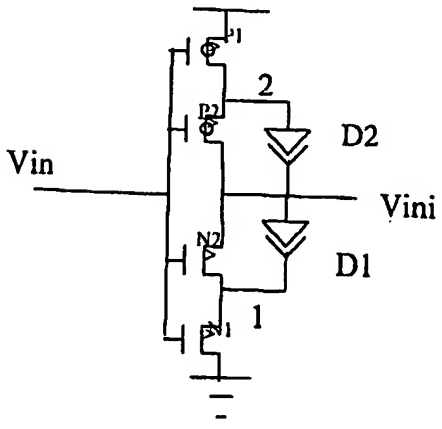
ZBUF

1. **Complementary clock**
2. **Cau add predriver stages for large output Transistors**
3. **50 ohm double terminated lines**
4. **Vtm = 0.6V**









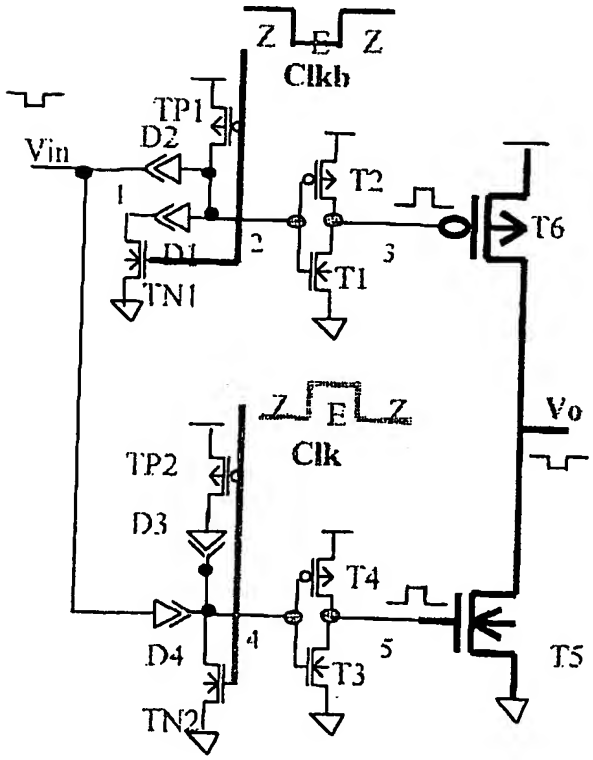
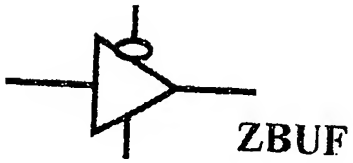
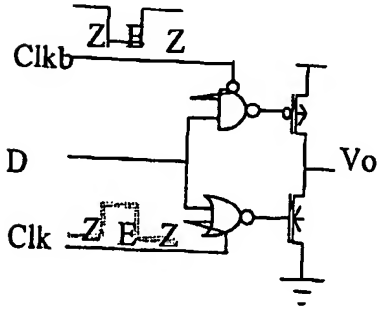


Fig. 12 ZBUF & Transceiver4 -SCL



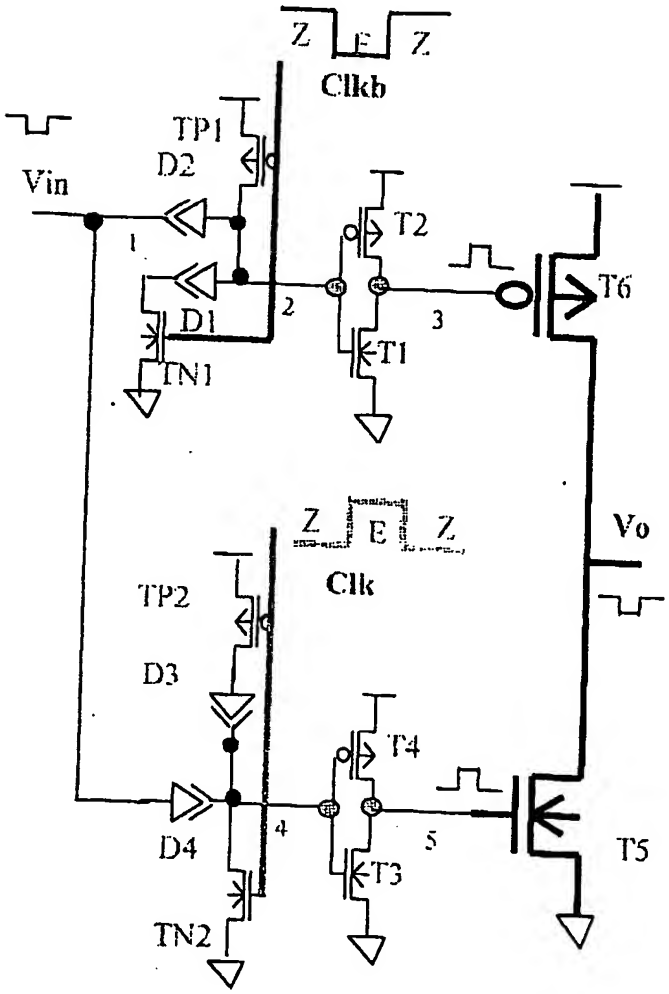
Vin	Clk	Clkb	Vo
X	L	H	Z
1	H	L	1
0	H	L	0

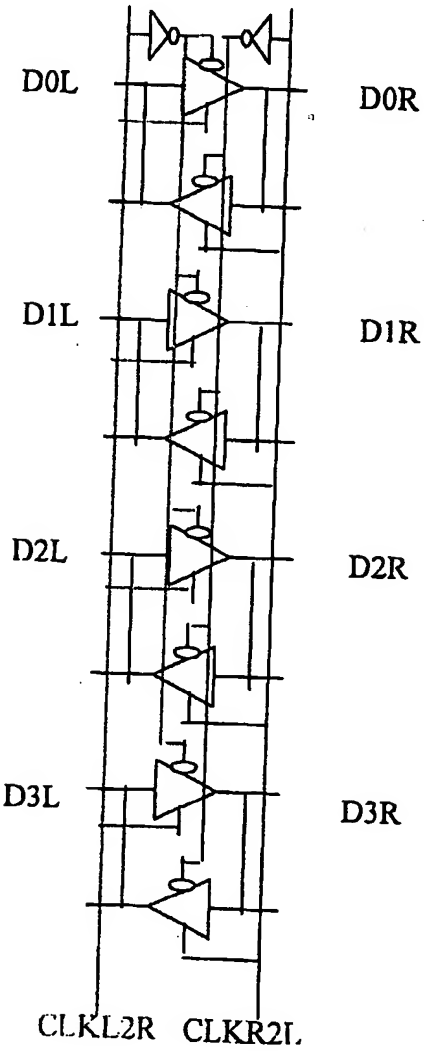


Clk and Clkb are complementary pairs

T1, T2 can scale up 3 stages to drive T6

T3, T4 can scale up 3 stages to drive T5





Hi Power GTLOBUF, Lo Power PDIBUF

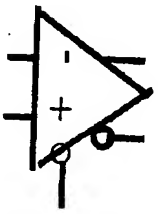
Fig. 13

GTL-OBUF

- Vcc =1.2V
- Vtm = 0.6V, Rtm = 25 ohm
- Voh = 0.8V
- Vol = 0.4V

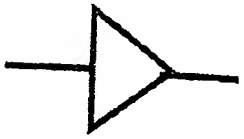
Pulsed DIFF IBUF

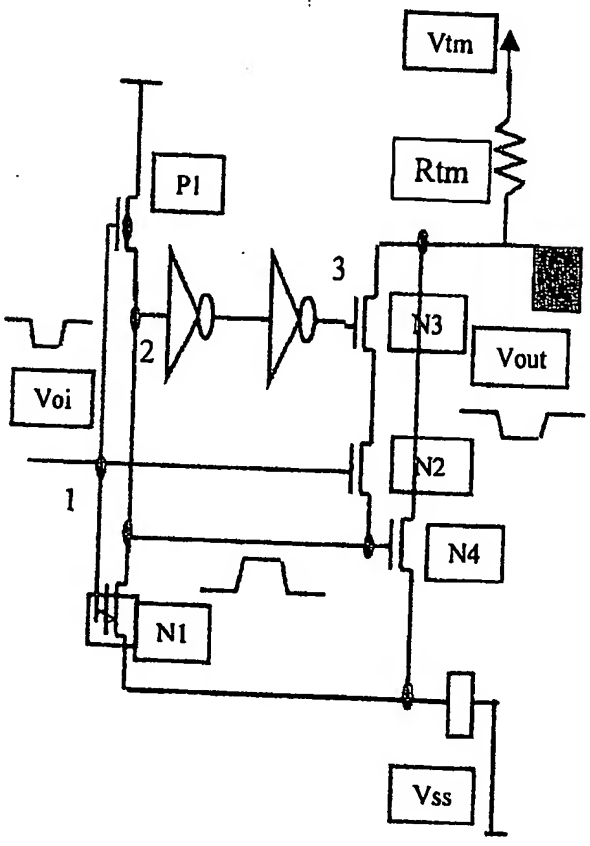
- Neg. CLKB
- DIFF input ~0.6V
- Single/Dual phase In/Output



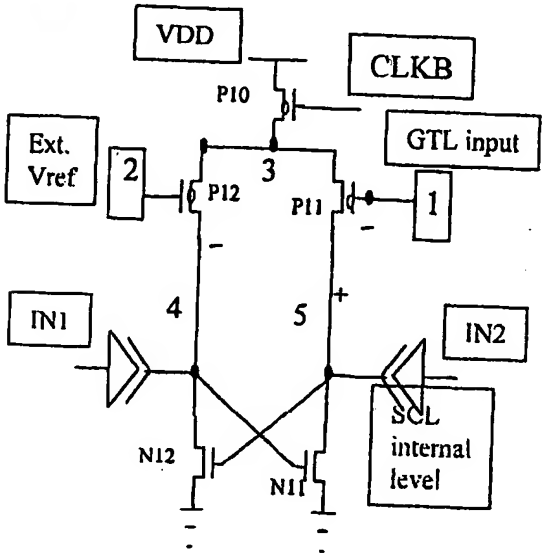
PDIBUF

GTOBUF



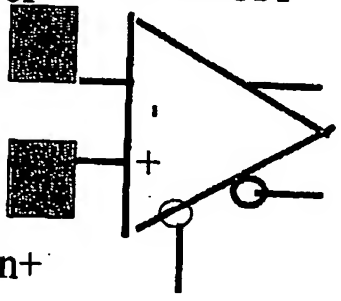


Dual Phase PDIBUFF



Vin-/
Vref

PDIBUFF



Vin1

Vin2

Vin+

Clkb

Fig. 14

- 常规CMOS-TTL方法

XOR2: W/O BUF

Transistor:	3 NTX 3PTX
Area/load units:	3 6
Tacc: ~150ps	2x (50:70:100),
effects: loading	Pre-dvr, current,

XOR4: W/O BUF

Transistor: 27	9 NTX 18PTX
Tacc: >800ps	3x (50:70:250),
effects: loading	Pre-dvr, current,

XOR4: W BUF

Transistor: 41	17 NTX 24PTX
Tacc: >400ps	3x (70:120:170),
effects: loading	Pre-dvr, current,

- GSD 解决方案: CMOS-DTL

XOR4: Build-in BUF

Transistor: 27	18 NTX 9PTX
Tacc: <200ps	2x (50:80:110), 4 times better
effects:	No ripple, No loading effect

Applications:

Packet switching: Preamble data stream check

Parity tree

Address change detection

Multi-phase PLL clock

...

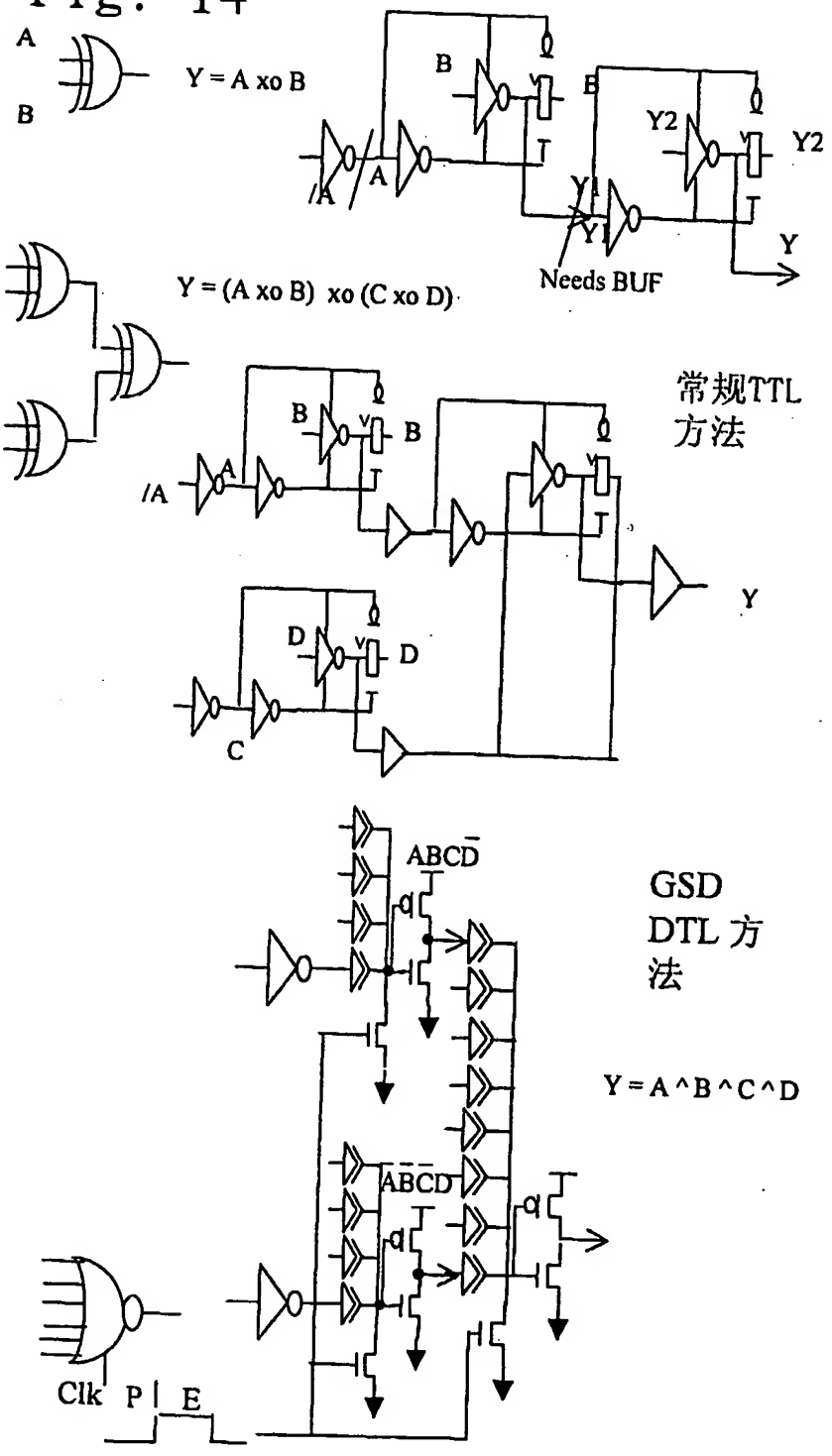
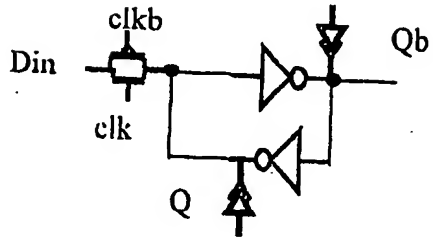
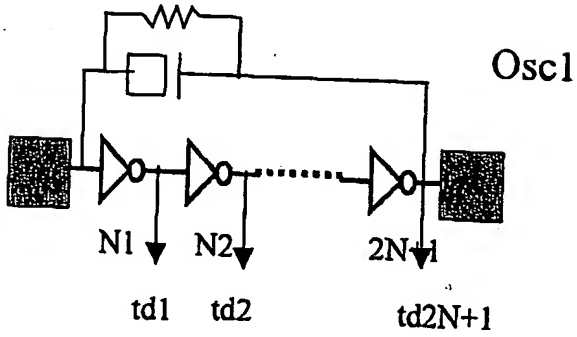


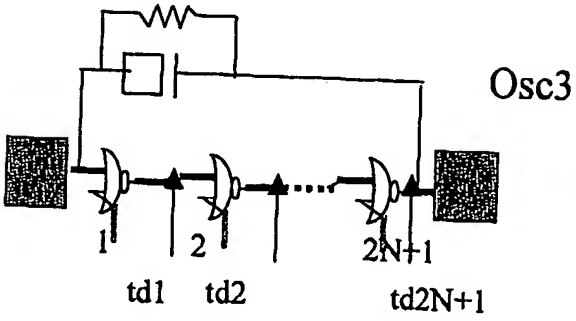
Fig. 15 Dlatch, Osc

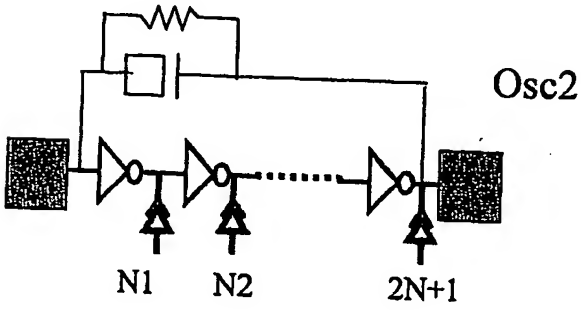
- Multivalued outputs
  - CMOS level
  - CML level

- CMOS Osc.: 2 Types
- SCL Oscillator/Delay taps
- Osc.: 2 types









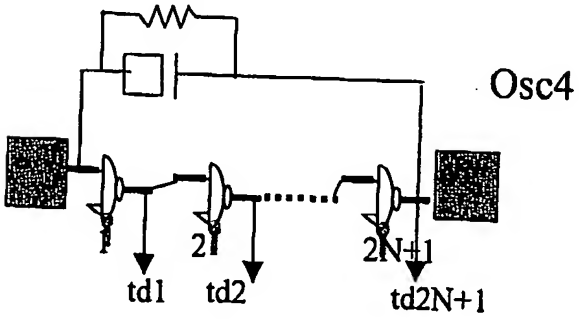
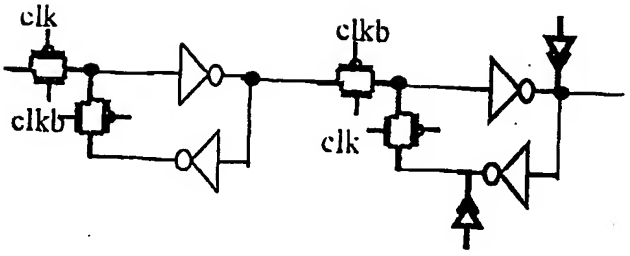
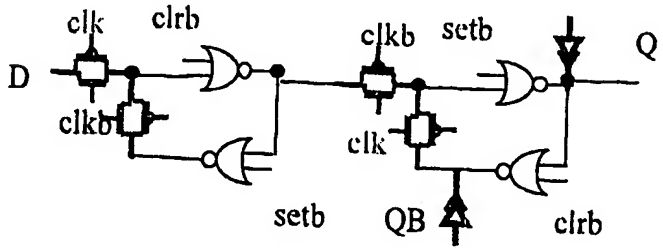
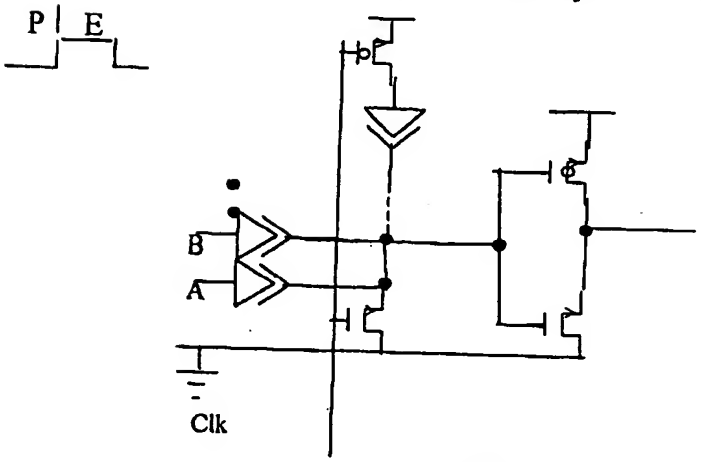


Fig. 16 GDFF-SCL



- Static DFF
- Set/Reset DFF
- SCAN register element





- Serial IN Parallel Out Shift Reg. - SIPOSR

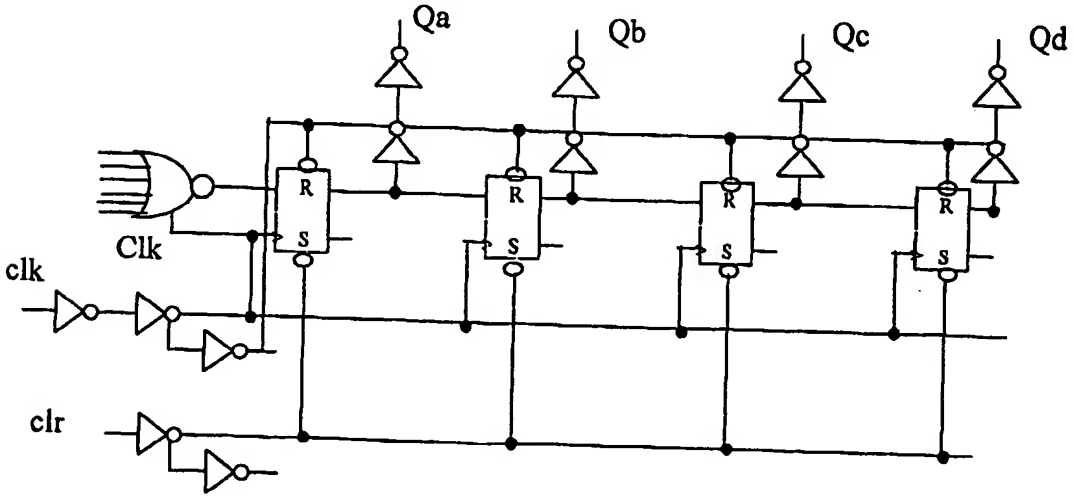
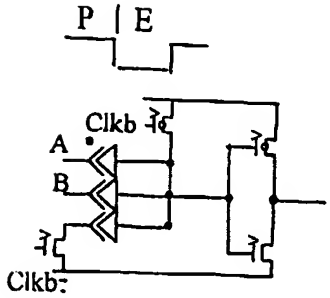


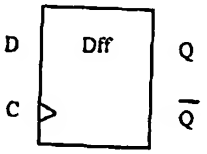
Fig. 17 DFF with GNAND

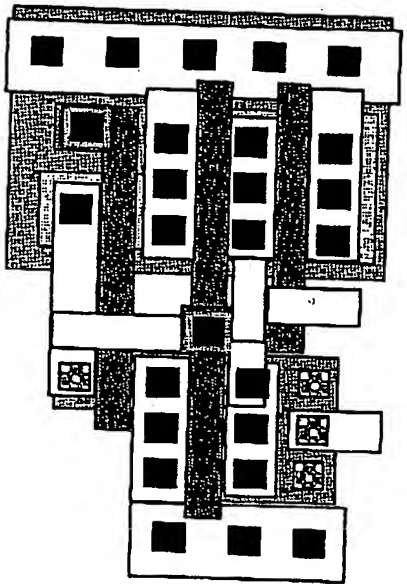
- GNAND Approach
- 18 Smaller Transistors

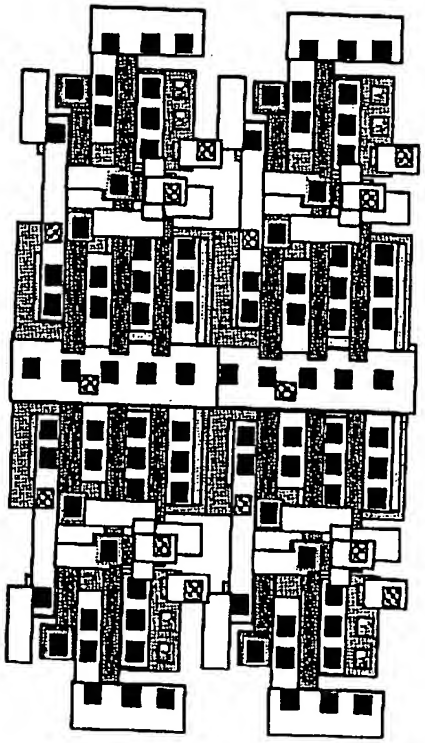
常规方法

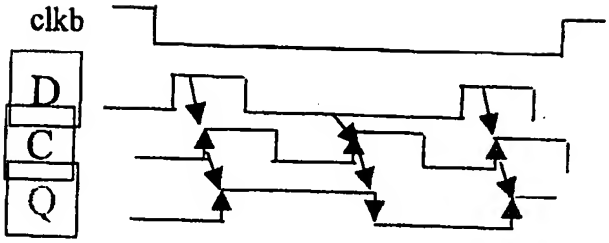
- **CMOS TTL , 22 txs**
- 2 phase clock
- **Slow serial pass Tx**
- **Scanable**











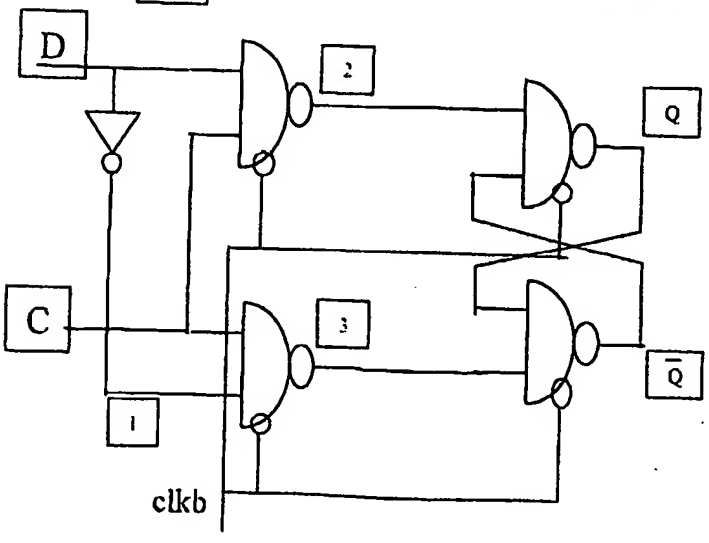
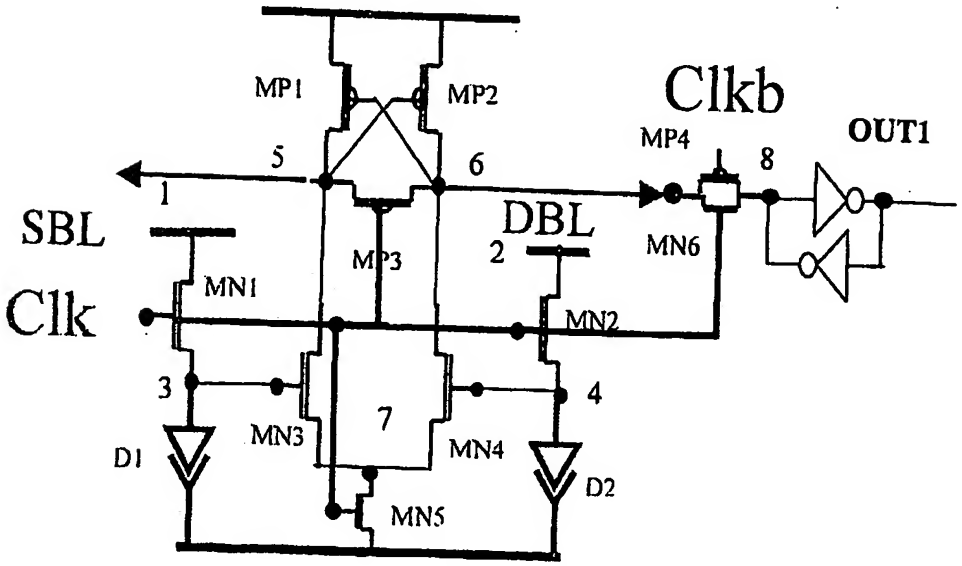
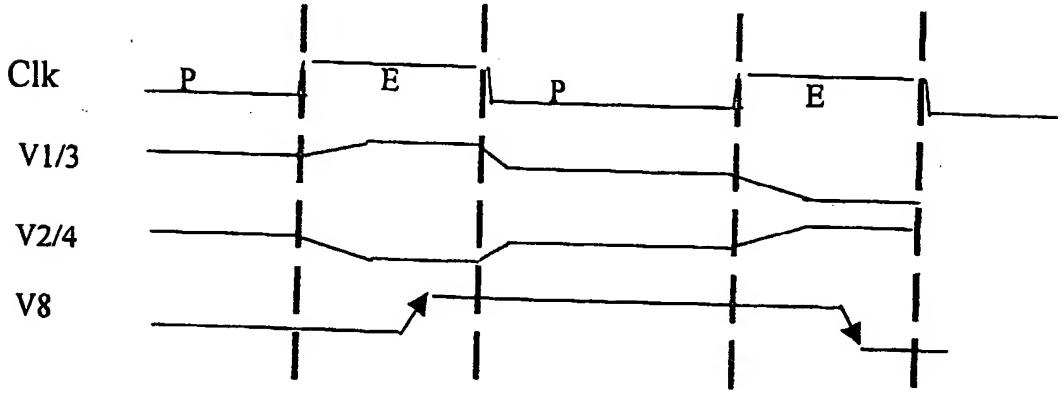


Fig. 18 IOBUF/Sense Latch

Dual Phase Dynamic Sense Amp

- Hi Embedded Resistance with D1, D2
- Diff Inputs may be V3, V4
- Diff Inputs may be V2, V2





Sense Amp Operation

Precharge: D1, D2 clamp MN3,4,5 OFF.

Evaluate: V3,4 pulsed on>>MN3,4,5 turned on>>MP1,2,3 Latching>>Output Latch reset

Fig. 19 Dual Ports

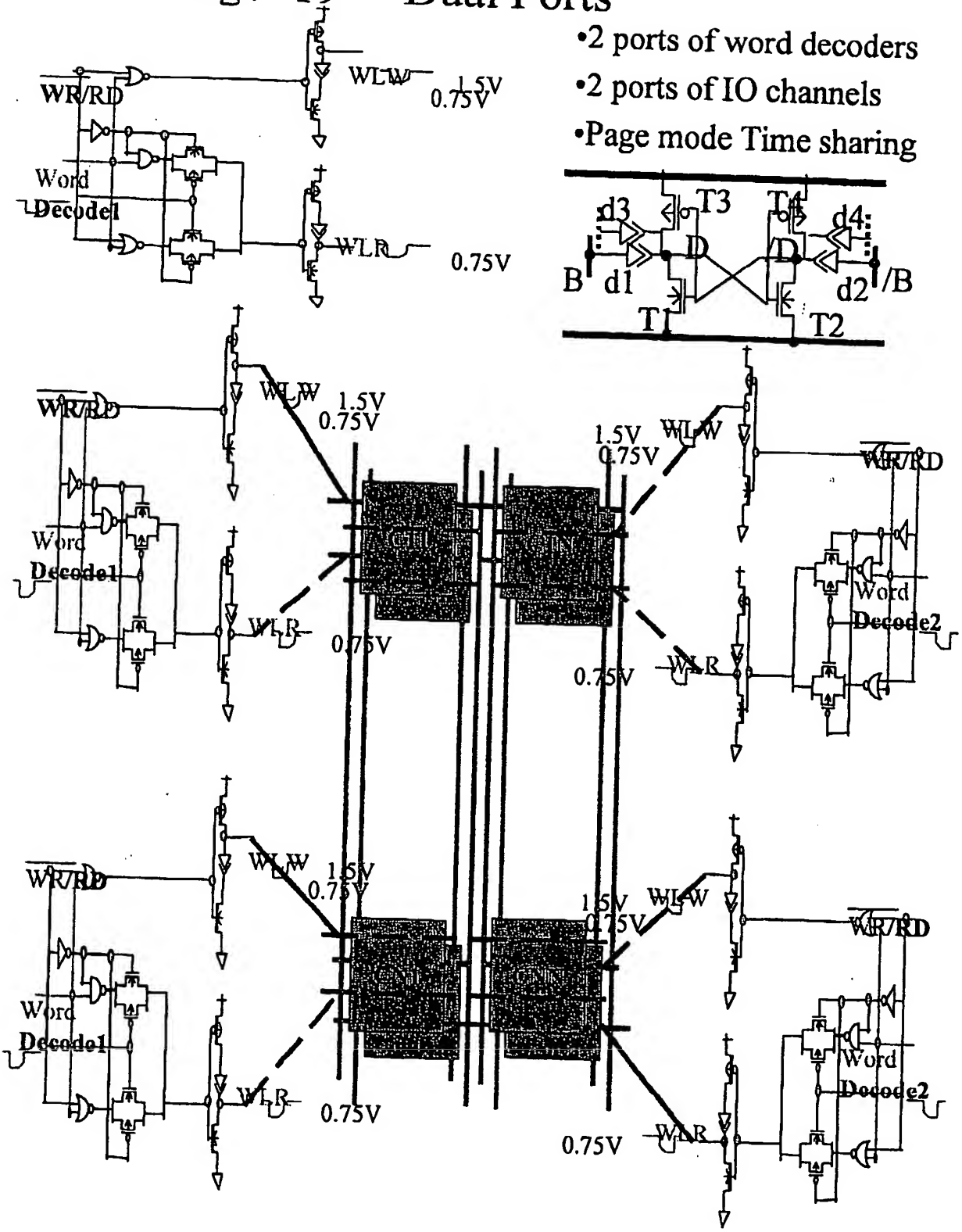


Fig. 20

Dynamic Read Only Memory-Hard and FPGA

DSP-Translation Lookaside Buf for coefficients

Controller- Microcode instructions

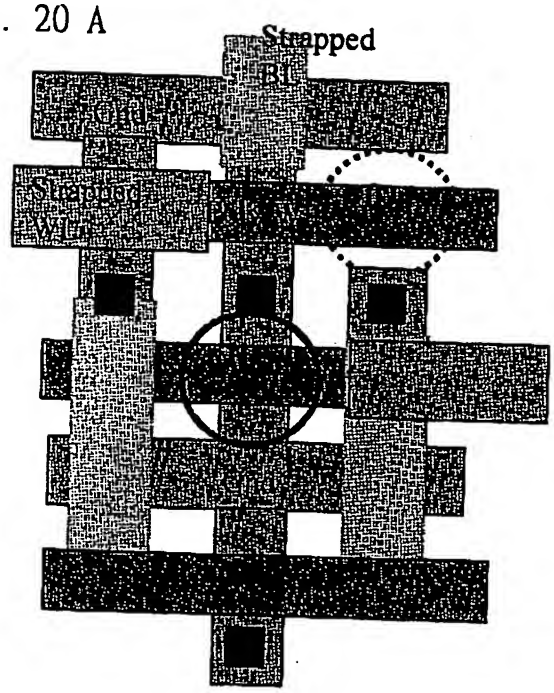
Tx Array : Dif Poly Defined

- **Common Gnd**
- **Shared Drain Contact**
- **Strapped M2 WL**
- **Pre-charged M1 BL**

Schottky array-Double density, low cost, high speed

- Vertical SBD, buried N+ cathode lines, with strapped M2 option.
- Pulsed decoder, M1 Word linel, No Poly

Fig. 20 A



Conventional CMOS Transistor ROM

Fig. 20 B

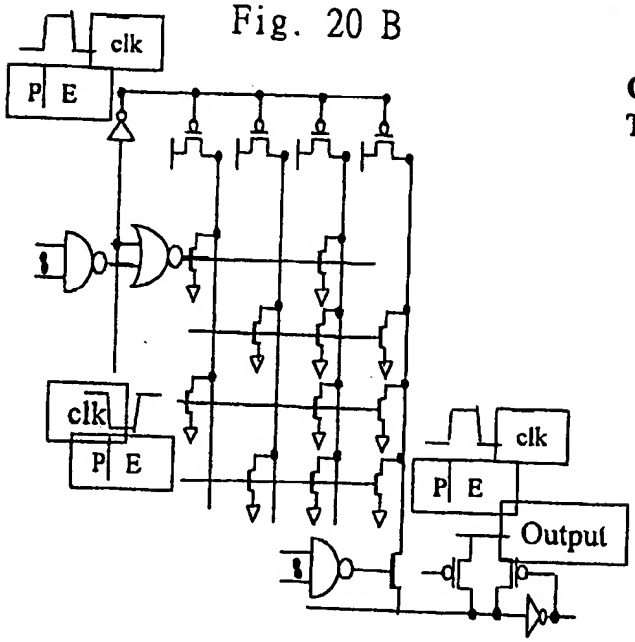


Fig. 20
Dynamic Read Only Memory-Hard and FPGA

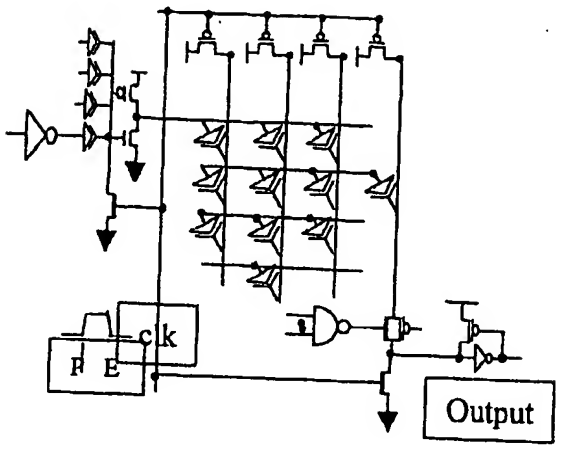
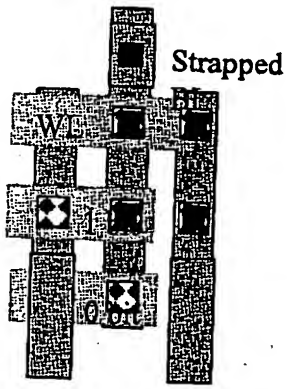


Fig. 20 C



SCL Dynamic SBD
ROM-Double Density
Faster Access times
Mask prog.

Fig. 20 D

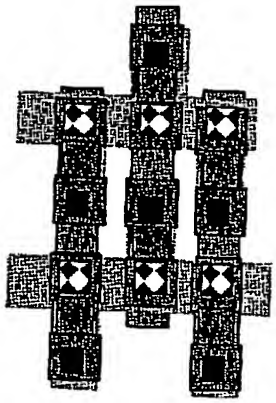


Fig. 20 E

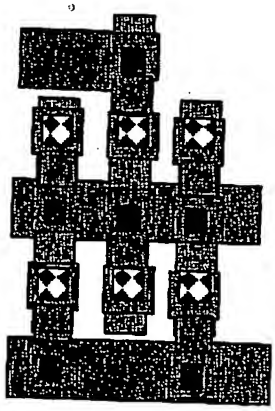


Fig. 20 F

SCL Dynamic SBD
ROM-Double Density
Faster Access times
Field prog.

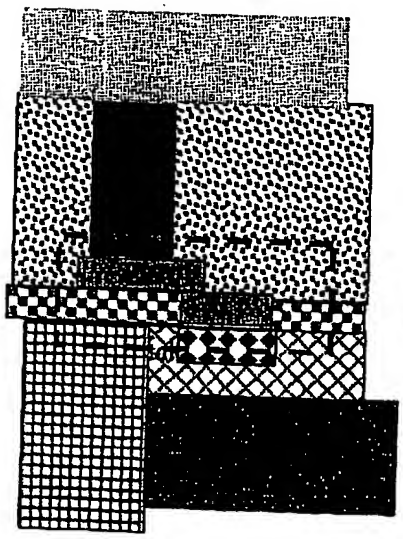


Fig. 20 G

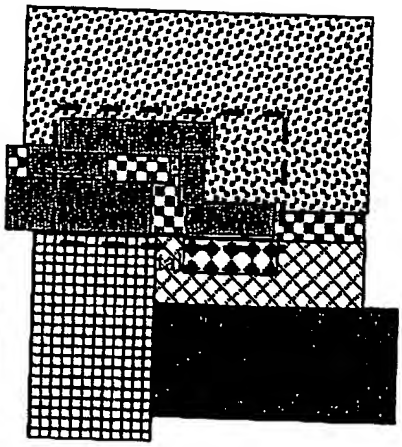


Fig. 20 H

Two schemes to make fuses of Local Interconnect

Legend

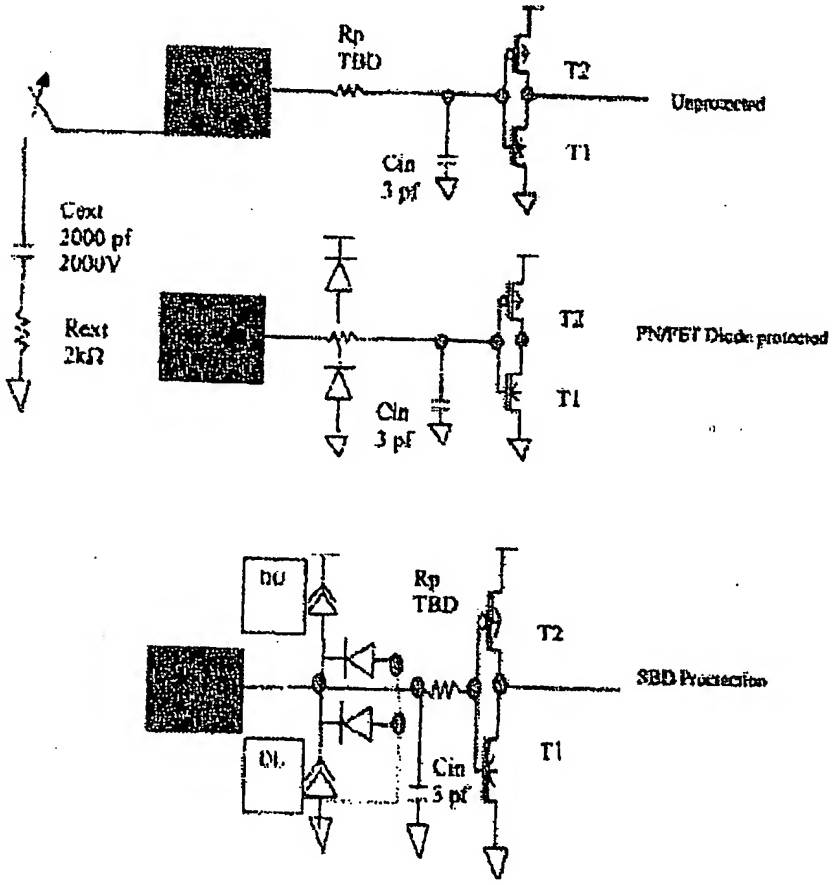
- LI film
- Poly contact
- Polycide
- 1st Metal
- 1st Metal plug
- Barrier metal
- N- cathode region
- N+ cathode region
- SiO2

ESD Input protection with SBD

Fig. 21

Input protection circuits

- High lead-in poly resistors > 100 kohm
- Limit current peaks to < 50 mA
- Conductive SBD and bipolar PN parasitics
- Low Cin < 1-3 pF



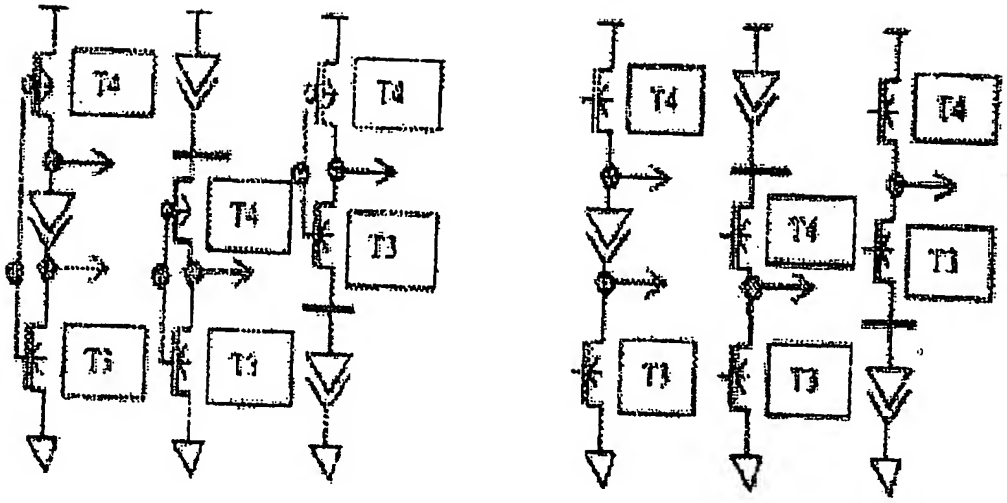


Fig. 22, Totem pole level shifting and Vref schemes with SBD string

Unprotected and protected P/Nwells

- Area of impact
  - IO cells
  - Array array: logic and Flash beds
- Parasitic device model
  - NPN in Pwell and PNP in Nwell
- Latch up due to lateral PNPN actions
- Suppression by passive N/Pwell tapping
  - Double ring big areas,
  - less margin
- Suppression by active device tapping
  - Suppress NPN by SBD in NMOS bed-biasing to GND
  - Suppress PNP by SBD in PMOS bed-biasing to VCC

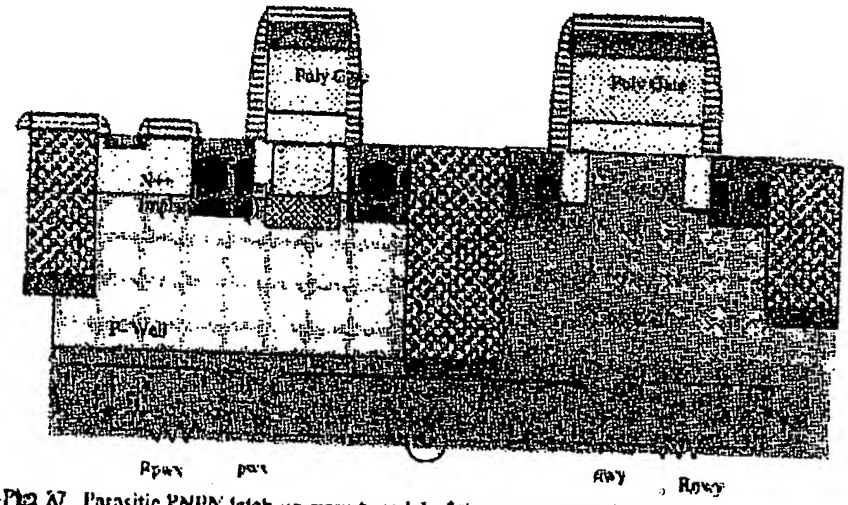


Fig. 23A Parasitic PNPN latch-up circuit model of the unprotected CFET transistors

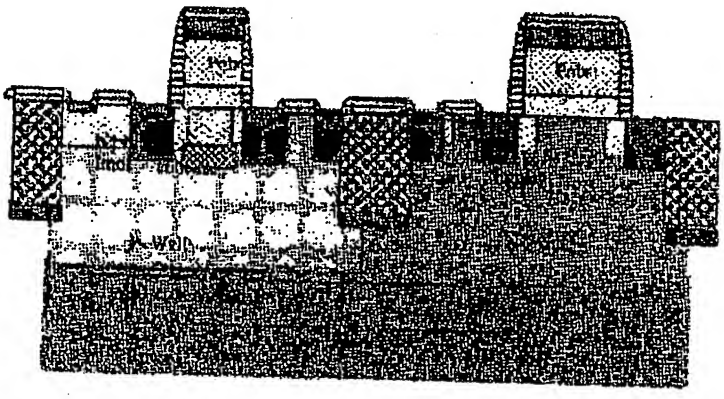


Fig. 23B add local active low barrier SBDs as needed

Input protection Circuits

Latch up protection, Fig. 22C

- Wire SBD in Nwell bed to VCC
- Wire SBD in Pwell bed to GND

Controlled Hot well biasing by SBD, Fig. 23

- Lower Vt

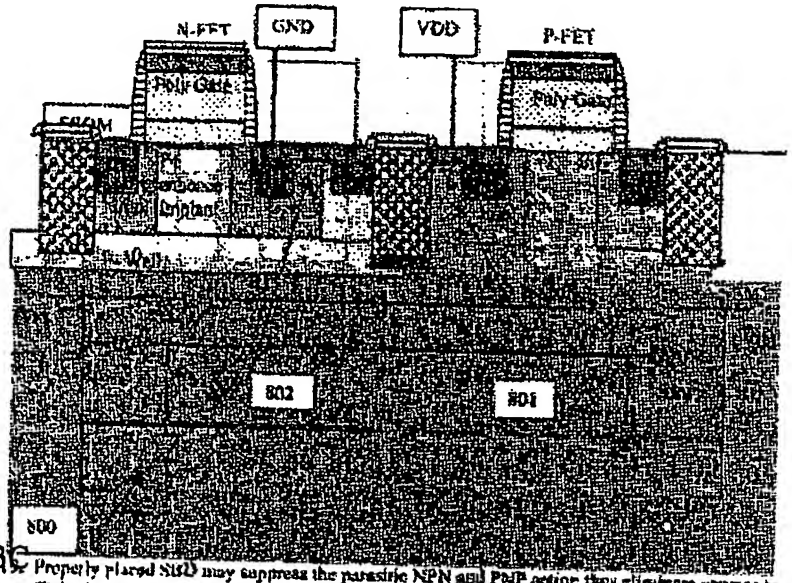


Fig. 23C

Fig. 23C Properly placed SBD may suppress the parasitic NPN and PNP action thus eliminate sources to latch-up. This circuit configuration may also forward bias the wells and lowering Vtn or Vtp.

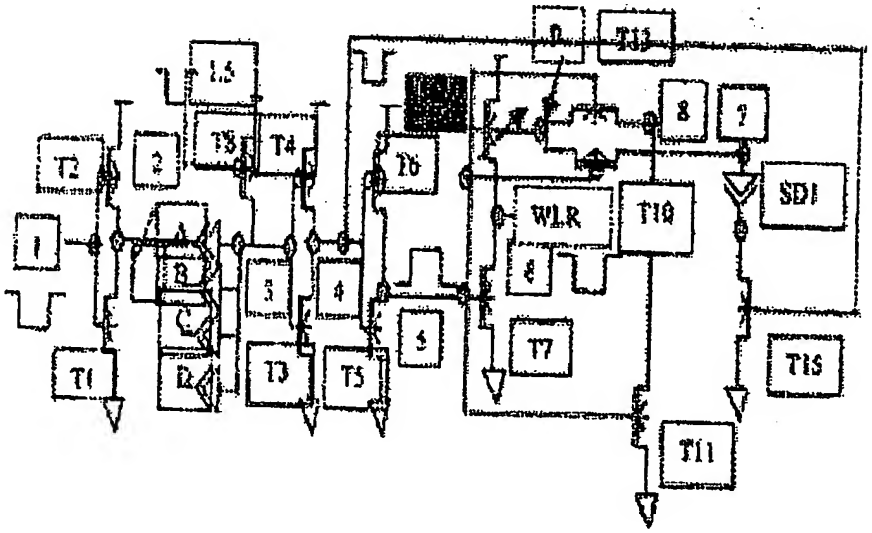


Fig. 20D LW driver NFET (T9) having dynamic Vtn.